GW5A-60K POWER SPEC

Name	Description	Min.	Max.
FPGA Logic			
V_{CC}	Core voltage, LV	0.93V	1.03V
	Core voltage, EV	1.14V	1.89V
V_{CCIO}	I/O Bank voltage	1V	3.465V
V_{CCX} [1]	Auxiliary voltage	1.71V	3.465V
V_{EFUSE} [2][3]	Voltage required for eFuse writing	1.62V	1.98V
MIPI			
V_{DDAM}	Analog core power supply voltage	0.87V	1.08V
V_{DDXM}	Analog auxiliary power supply voltage	1.71V	3.465V
V_{DDDM}	Digital core power supply voltage	0.87V	1.08V
V_{DD12M}	MIPI LP power supply voltage	1.14V	1.32V
ADC			
$V_{CCLDOADC}$	Power supply voltage of internal LDO module that provides voltage for ADC	1.71V	1.89V
V_{CCADC}	ADC power supply voltage	1.62V	1.98V
V_{REFN}	ADC reference voltage	0V	0V
V_{REFP}	ADC reference voltage	0V	1.25V

Note!

[1] When internal differential termination resistors are required, Vccx must be greater than or equal to 3V; the IO input-output Fmax is limited when Vccx=1.8V, and Vccx needs to be greater than or equal to 2.5V for input-output applications with Fmax greater than 600Mbps.

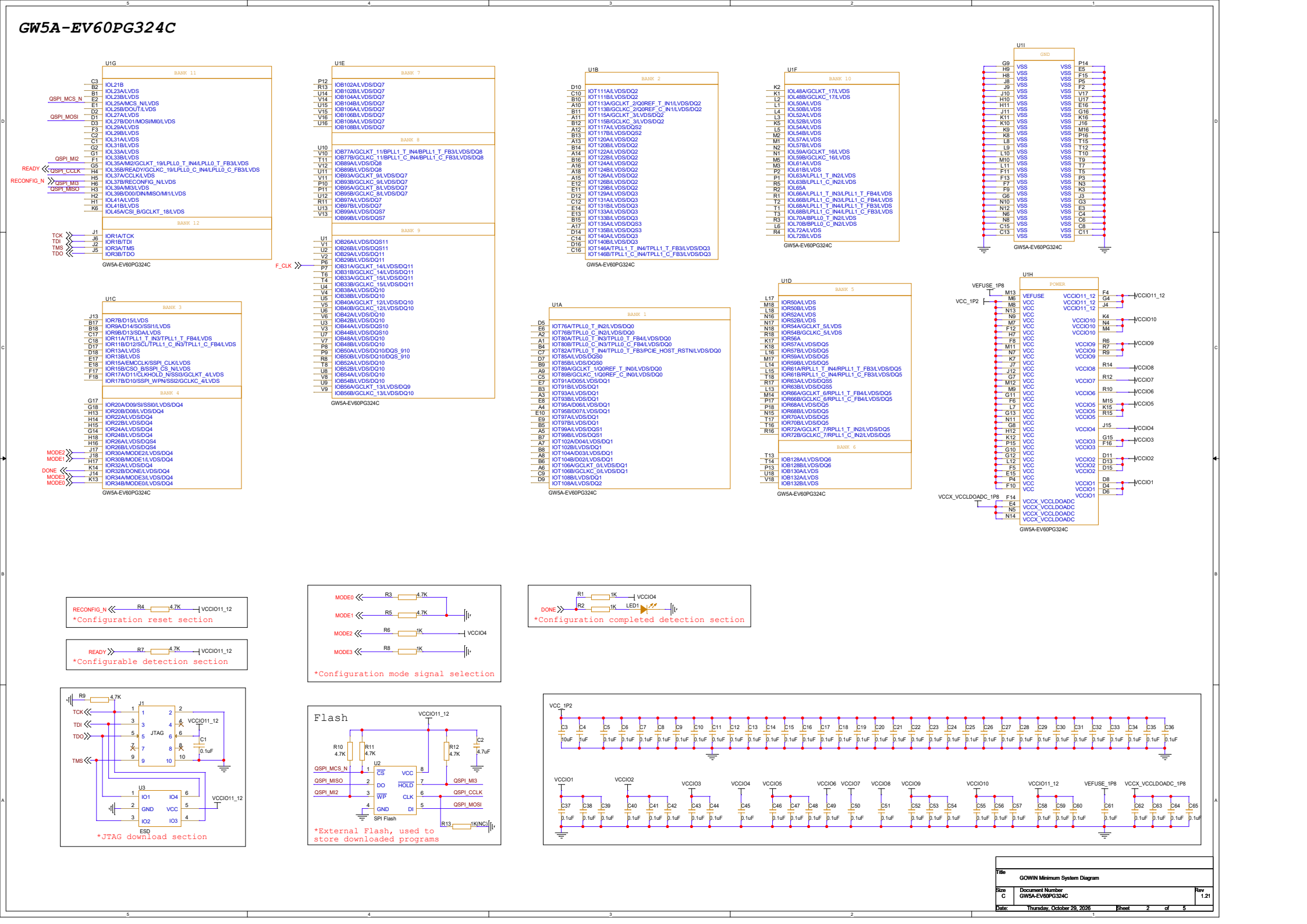
[2] When V_{EFUSE} programming is not required, this power supply can be connected to GND or left floating.

[3] When V_{EFUSE} programming is required (e.g., for programming AES key, changing the boot address of Multiboot related golden image, etc.), confirm that the V_{EFUSE} voltage is set to 1.8V.

If multiple power supplies are shorted on some packages or PCBs, it is necessary to take the intersection of the ranges of all shorted power supplies to satisfy the needs of multiple power supplies at the same time.

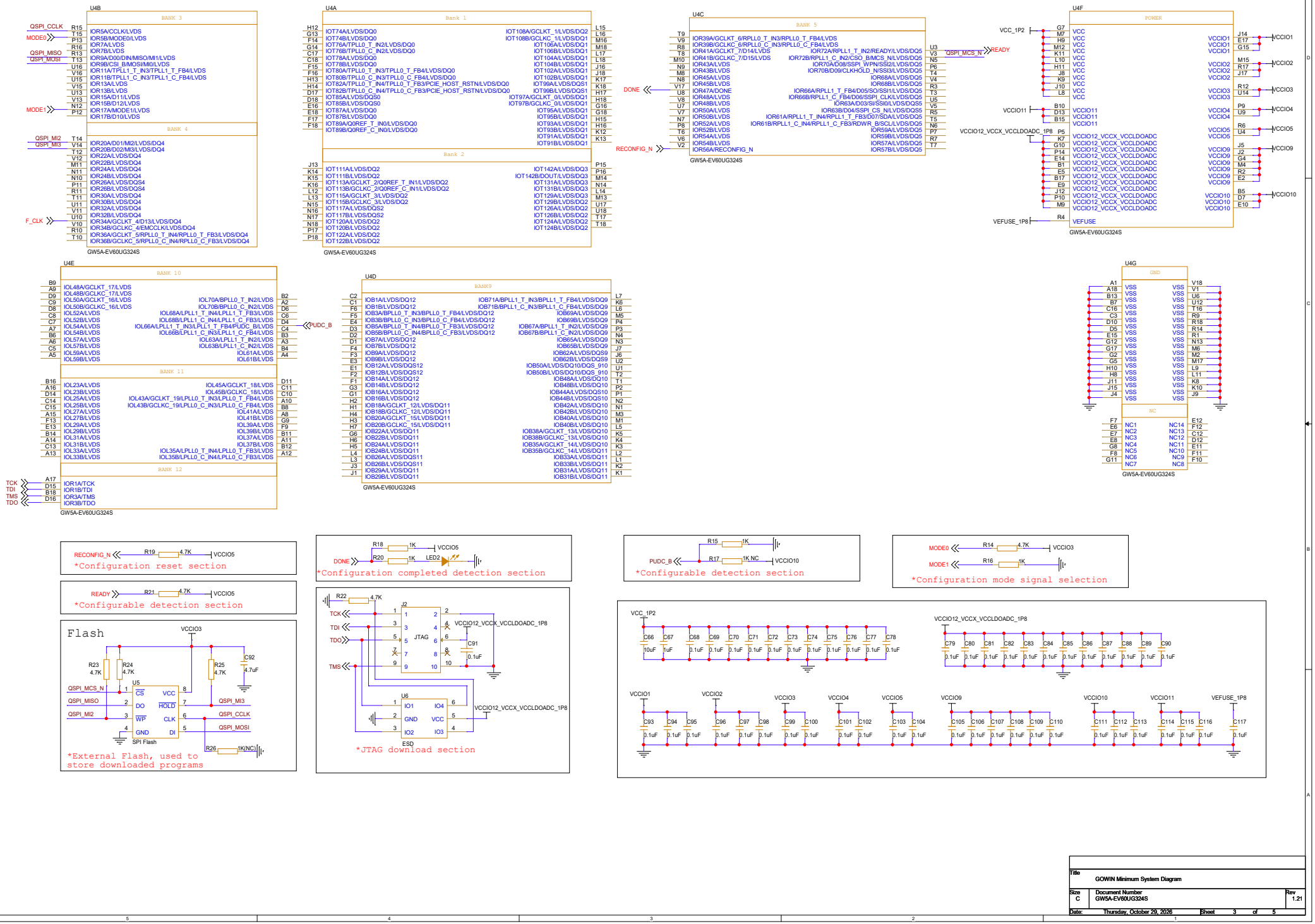
Notes:
1.F_CLK signal is an external input clock signal.
  It is recommended that F_CLK signal be provided through an active oscillator crystal.
2.External Flash memory is used to store downloaded programs.
For details about SPI Flash model selection, see "Chapter 4.5 SPI Flash Selection" in UG718,
Arora V 60K FPGA Products Programming and Configuration Guide .
3.It is recommended that add an ESD protection chip to the JTAG download circuit.
4.VCC core voltage requires a large current, so it is recommended to supply power separately.
5.The MODE pin is the GowinCONFIG configuration mode selection signal.
For details about how to select the Mode signal, see "Chapter 3.1 Configuration Modes" in UG718,
Arora V 60K FPGA Products Programming and Configuration Guide.

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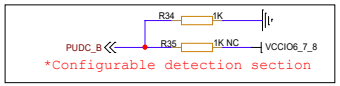
GW5A-EV60UG324S

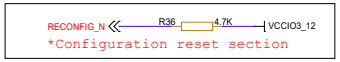


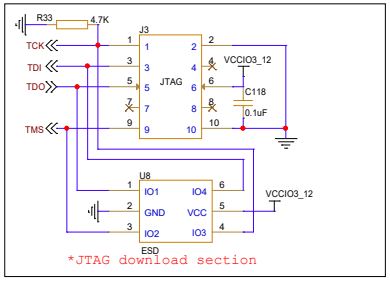
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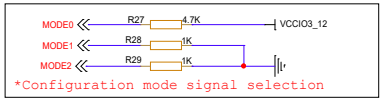
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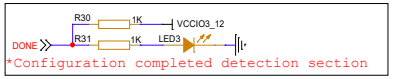


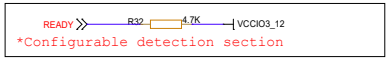


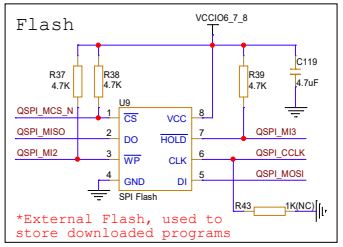


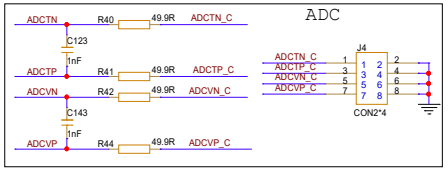


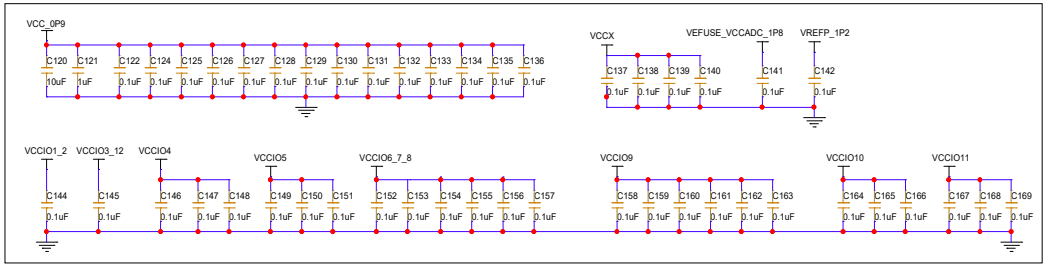








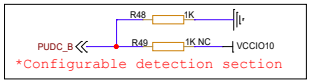


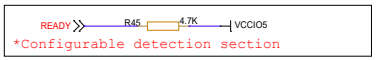


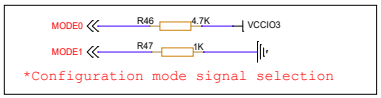
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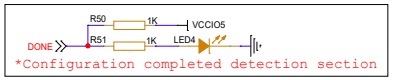
GW5A-LV60UG324S

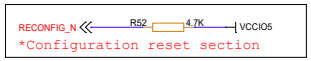


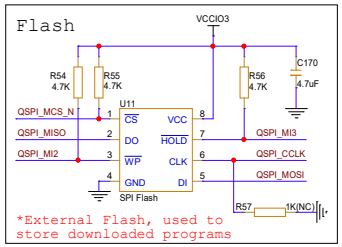


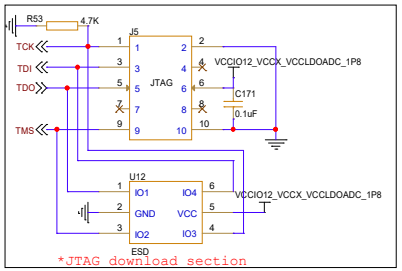


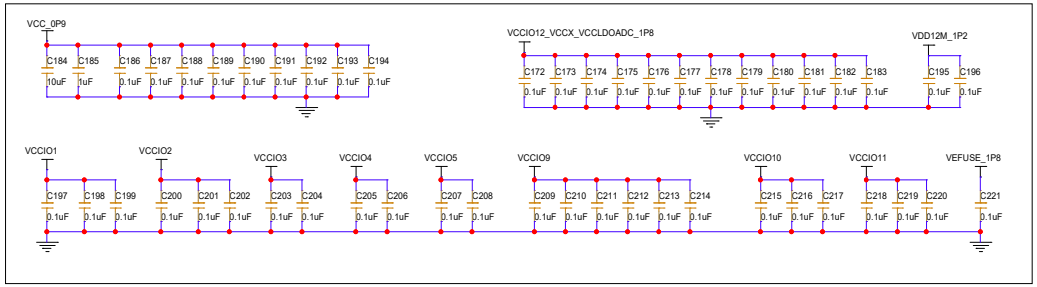












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